以單光子陣列為基礎的影像擷取晶片設計與應用(3/3)

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計畫目標

研發新一代單光子陣列感測晶片

- 開發單光子擷取成像技術
- 有效提升感測裝置時間與空間的解析度
- 提高影像擷取速度

台日美三國專利申請:

- 台灣:具深度資訊之影像感測晶片 (申請案號:第111140148號專利申請案)
- 美國:IMAGE SENSORS CHIP WITH DEPTH INFORMATION (申請案號:18/191,714)]
- 日本:深度情報を有したイメージセンサチップ (申請案號:2023-093602)

執行成果重點摘要

Single Photon Avalanche Diode (SPAD)

晶片產出: 採用台積電 0.18um CMOS 高壓製程

- SPAD Imager (1st year: 3 chips, 2nd year: 2chips)
- TDC (1 chip)

超高速影像擷取平台: 建立光路與高速、高解度量測平台

國際合作:與 Stanford/SLAC 團隊共同研究單分子運作機制, 參與朱棣文院士 NIH 的四年研究計畫

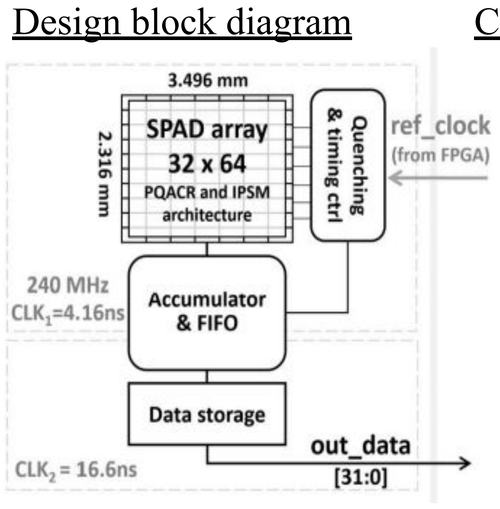
論文七篇:

- **Chun-Chi Chen**, Yun-Sheng Chan, Yu-Hao Fang, Yun-Ming Wang, and **Chen-Yi Lee**, "Rapid Portable Electrical Biosensing Design with Dielectrophoresis and its Applications for Cardiac Biomarker Detection", IEEE Sensors Journal, Vol. 20, No. 16, Aug. 15, 2020, pp. 8981-8989.
- **Eugene Lee** and **Chen-Yi Lee**, "Smart Wearable Devices with Energy-Efficient Computing for PPG-based Mobile Health-Care Applications", IEEE Sensors Journal. Vol. 21, No. 12, June 15, 2021, PP. 13564-13573.
- **H.-H. Huang, C.-H. Liu, T.-Y. Huang, S.-D. Lin, and C.-Y. Lee**,"Self-Restoring and Low-Jitter Circuits for High Timing-Resolution SPAD Sensing Applications," presented at the 2023 IEEE ISCAS, May, 21-23 2023.
- **T.-Y. Huang, H.-H. Huang, C.-H. Liu, S.-D. Lin, and C.-Y. Lee**, "Stack-Based In-Pixel Storage Circuit for SPAD Photon Counting," presented at the 2023 IEEE ISCAS, May, 21-23 2023.
- **H.-H. Huang, T.-Y. Huang, C.-H. Liu, S.-D. Lin, and C.-Y. Lee**,"32x64 SPAD Imager Using 2-bit In-Pixel Stack-based Memory for Low-Light Imaging", accepted by IEEE Sensors Journal on 07/23/2023, DOI: 10.1109/JSEN.2023.3299276
- **H.-H. Huang, T.-Y. Huang, C.-H. Liu, S.-D. Lin, and C.-Y. Lee**,"A Dual-Mode Readout Circuit for SPAD Imaging Applications", submitted to IEEE TCAS II.
- **T-Y. Huang, P-Y. Huang, and C-Y Lee**, "A Low-Latency Data Compressor for SPAD-Based Depth Estimation Systems", submitted to IEEE TCAS II

SPAD G2.1 target application: low-light imaging

Speculation: 4 photons within 120ns, Fill factor >10%,
Continuous photon counting
Frame rate : 117 kfps

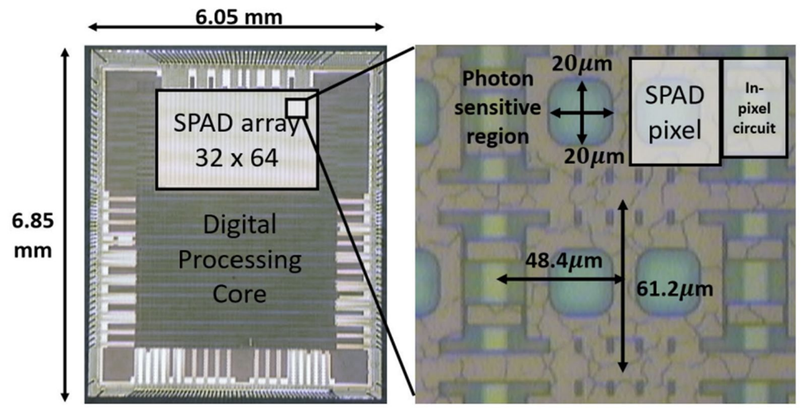
Design block diagram



Chip summary

Property	Measurement
Technology	180nm
Chip area (mm^2)	6.05 x 6.85
SPAD array size	32 x 64
Peak PDP (%)	57
Median DCR (cps)	810
Event rate (bps)	61.4G
Frame rate (fps)	117k

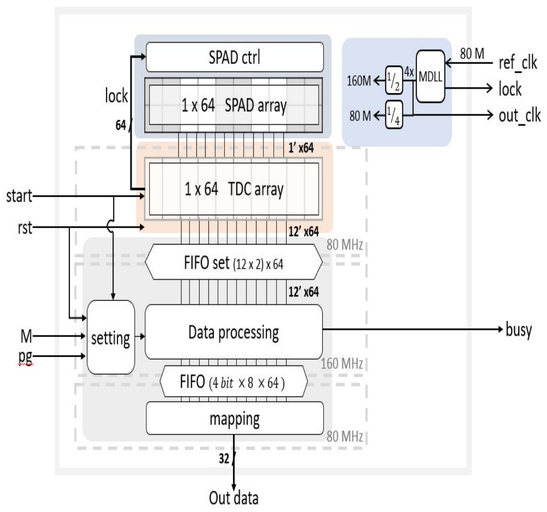
Micrograph of chip and SPAD



SPAD G3.1: target application d-TOF

Speculation: 1 photon within 230ns, Data compression, Fill factor > 35%
Global shutter
Event rate: 311 Mcps @75Hz

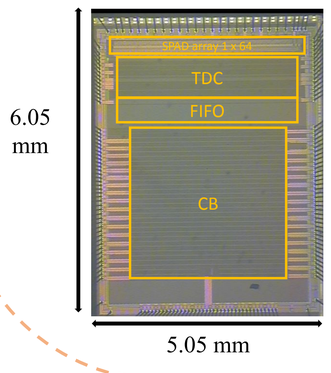
Design block diagram



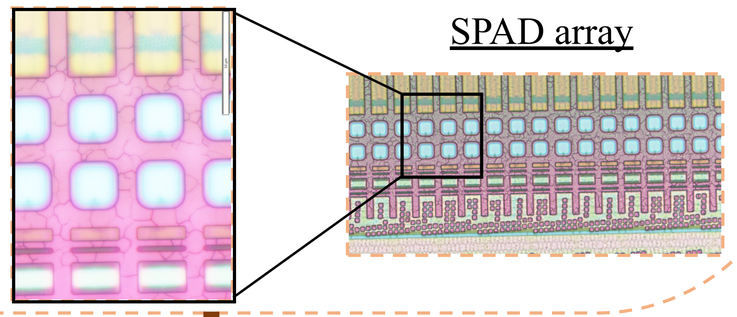
Chip summary

Property	Measurement
Technology	180 nm
Chip area (mm^2)	5.05 x 6.5
TDC area (mm^2)	4.3 x 0.35
TDC power	310 mW
TDC resolution	55 ps
Range	230 ns
TDC P-P variation	< 0.01%
SPAD array size	1 x 64 Pixel (4 SPAD/Pixel)
SPAD DCR (Hz)	208 @ 2 V(1 SPAD)
Power (digital)	345 mW @150 MHz, 1.92 V
SPAD fill factor	38%
Event rate	311 Mcps @75MHz

Micrograph



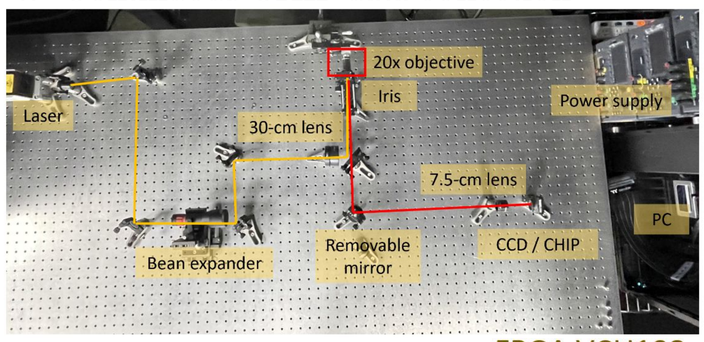
SPAD array



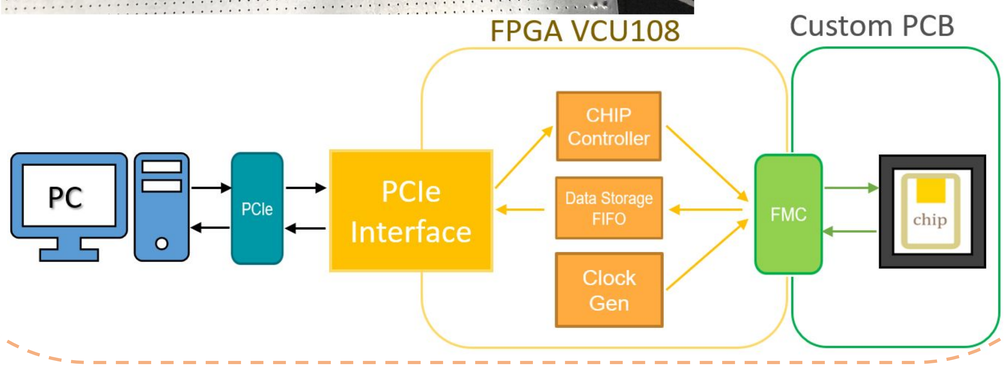
SPAD Imaging System Platform

Speculation:

1. FPGA-constructed CHIP data transmission system
2. User defined observation time for smFRET and FLIM system
3. High data throughput using PCIe interface
4. Continuous CHIP data collection



Sample



Prototype System: Optical Platform Demo

Image of Convallaria majalis rhizome stained with acridine orange (Cell Wall)