以單光子陣列為基礎的影像擷取晶片設計與應用(2/3)

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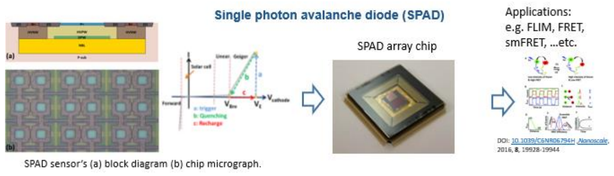
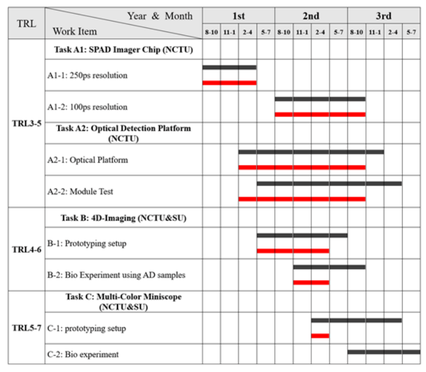
計畫目標

研發新一代單光子陣列感測晶片

- 開發單光子擷取成像技術
- 有效提升感測裝置時間與空間的解析度
- 提高影像擷取速度





執行成果重點摘要

Single Photon Avalanche Diode (SPAD)

晶片產出: 採用台積電 0.18um CMOS 高壓製程

- SPAD Imager (1st year: 3 chips, 2nd year: 2chips)
- TDC (1 chip)

超高速影像擷取平台: 建立光路與高速、高解度量測平台

國際合作: 與Stanford/SLAC團隊共同研究單分子運作機制, 參與朱棣文院士NIH的四年研究計畫

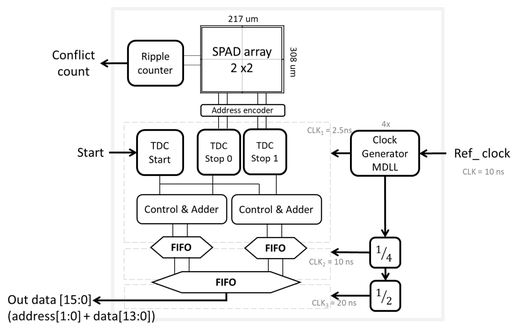
論文三篇:

- **Chun-Chi Chen**, Yun-Sheng Chan, Yu-Hao Fang, Yun-Ming Wang, and **Chen-Yi Lee**, "Rapid Portable Electrical Biosensing Design with Dielectrophoresis and its Applications for Cardiac Biomarker Detection", IEEE Sensors Journal, Vol. 20, No. 16, Aug. 15, 2020, pp. 8981-8989.
- **Eugene Lee** and **Chen-Yi Lee**, "Smart Wearable Devices with Energy-Efficient Computing for PPG-based Mobile Health- Care Applications", IEEE Sensors Journal (Accepted).
- **Hsi-Hao Huang**, Tzu-Yun Huang, Chun-Hsien Liu, Yan-Kai Tzeng, Steven Chu, Sheng-Di Lin, and **Chen-Yi Lee**, "A 32X64 SPAD Imager Using Stacked In-Pixel Memory with 40MHz Observation Rate for smFRET Applications", submitted to IEEE Sensors Journal

SPAD G2.5 + TDC G2

Speculation: SPAD integrated with TDC, Timing Resolution: <100ps

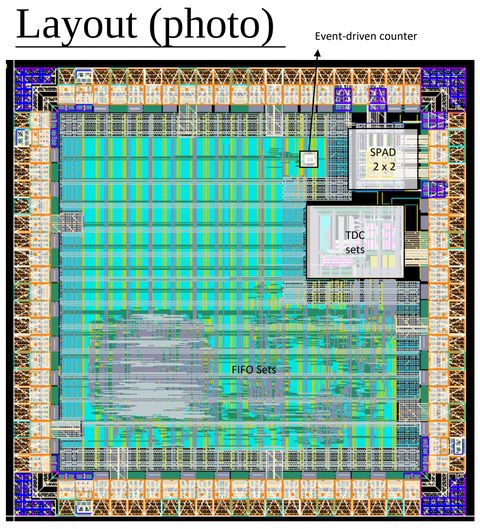
Design block diagram



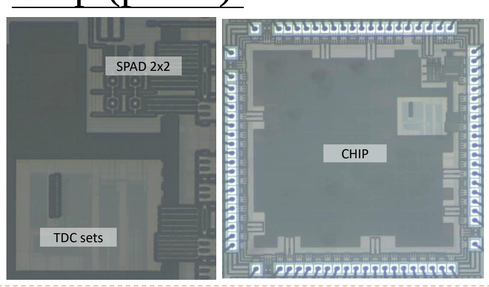
Chip summary

Property	Measurement
Max clock frequency	115MHz
Output port speed	57.5MHz
Timing resolution	87.23 ps
Pixel number	2 x 2
Chip size	2 x 2 mm^2
Aspect ratio	1.01
Fill factor	12.2%
Total Power	48.6 mW @80MHz, 1.8v

Layout (photo)



Chip (photo)



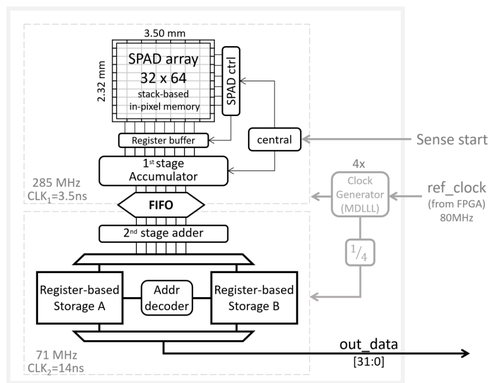
SPAD G2.1: target application FRET

Speculation: 4 photons within 120 ns, Fill factor > 10%

Continuous photon counting

Observation rate: 30Mfps

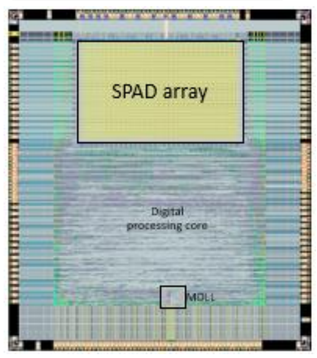
Design block diagram



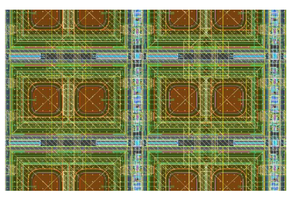
Chip summary

	G2	G2.1
Chip area (mm^2)	8.05 x 8.45	6.05 x 6.85
Peak power (digital)	2.25 Watt @208MHz, 1.8V	0.82 Watt @285MHz, 1.8V
Peak power (SPAD)	1.2 Watt	1.03 Watt
SPAD DCR(Hz)	>10k	<300
SPAD array size	32 x 64	
SPAD array area (mm^2)	4.02 x 2.46	3.5 x 2.3
SPAD fill factor	10.6 %	13.4%
1bit Frame rate (fps)	26M @208MHz	36M @285MHz

Layout (photo)



SPAD array



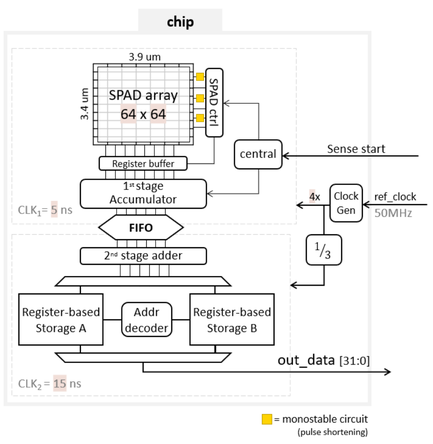
SPAD G1.1: target application FLIM

Speculation: Global Shutter, Fill factor > 10%

Timing Resolution: 1st year:<0.7ns / 2nd year: <100ps

Pixel Array: 64x64

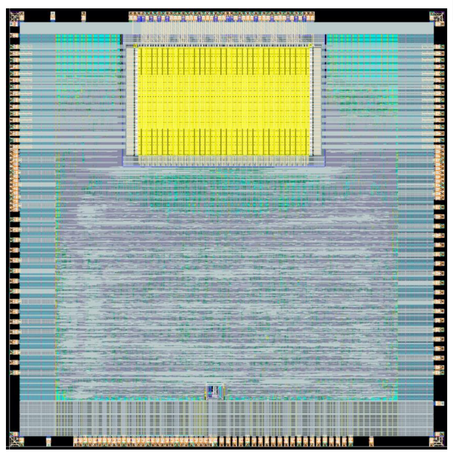
Design block diagram



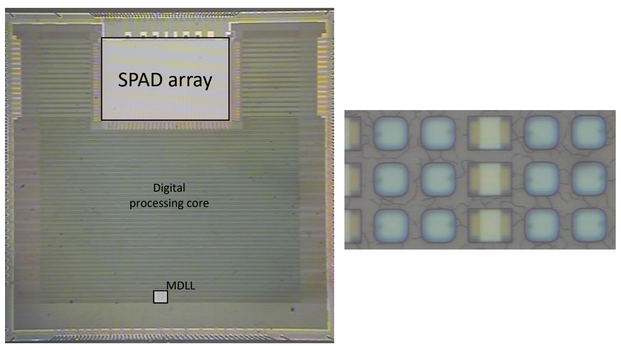
Chip summary

	G1	G1.1
Chip area (mm^2)	8.05 x 5.65	8.45 x 8.45
Peak power (digital)	2.01 Watt @208MHz, 1.8V	2.6 Watt @200MHz, 1.8V
SPAD DCR(Hz)	>10k	<300
SPAD array size	64 x 64	
SPAD array area (mm^2)	3.9 x 3.4	3.9 x 2.5
SPAD fill factor	20.77 %	17.4%
1bit Frame rate (fps)	3.1M @200MHz	16.6M @200MHz
Timing resolution	625ps	40ps
Exposure mode	Partial global shutter	Complete global shutter

Layout (photo)



Chip (photo)



SPAD Imaging System Platform

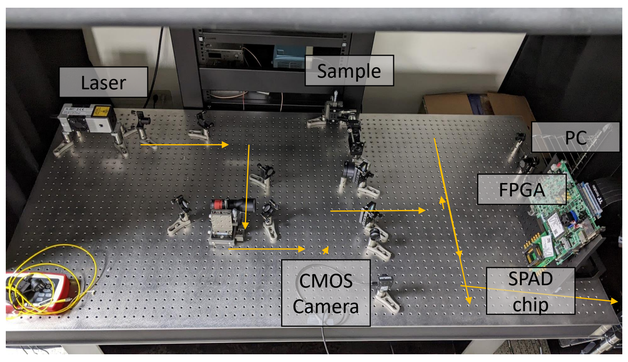
FPGA based data communication system

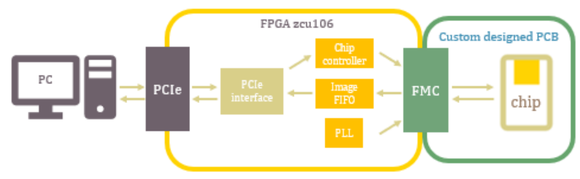
Speculation:

Continuous data transfer.

User defined observation time for smFRET and FLIM system.

High data throughput using PCIe interface.





SPAD Demo System: 10kHz chopper

Image of Convallaria majalis rhizome stained with acridine orange (Cell Wall)